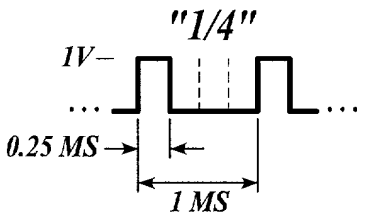


Fig. 1A

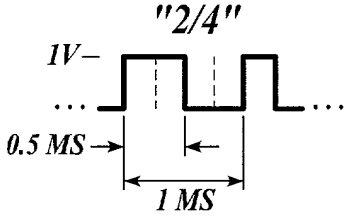


Fig. 1B

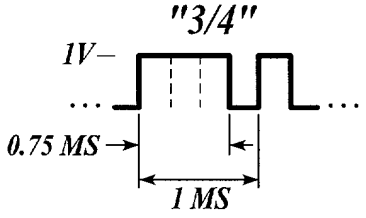


Fig. 1C

Fig. 2

NUMBER OF UNIT PULSE LENGTHS	MODULATOR BINARY OUTPUT COMBINATIONS	TIMER STATE	EFFECTIVE DUTY CYCLE
0	0 0 0 0	0 1	= 0% (0/8)
	0 0 0 0	0 1	
1	0 0 0 1	0 1	= 12.5% (1/8)
	0 1 0 0	0 1	
2	0 1 0 1	0 1	= 25% (2/8 = 1/4)
	0 1 0 1	0 1	
	0 0 1 0	0 1	
	1 0 0 0	0 1	
3	0 0 1 1	0 1	= 37.5% (3/8)
	1 1 0 0	0 1	
	0 1 1 0	0 1	
	1 0 0 1	0 1	
4	0 1 1 1	0 1	= 50% (4/8 = 1/2)
	1 1 0 1	0 1	
	1 0 1 0	0 1	
	1 0 1 0	0 1	
5	1 0 1 1	0 1	= 62.5% (5/8)
	1 1 1 0	0 1	
6	1 1 1 1	0 1	= 75% (6/8 = 3/4)
	1 1 1 1	0 1	

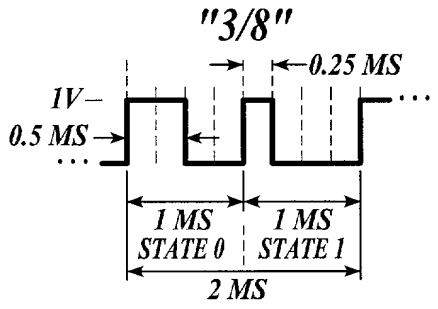

"3/8"
0.25 MS
1V
0.5 MS
1 MS
STATE 0
1 MS
STATE 1
2 MS

Fig.3A

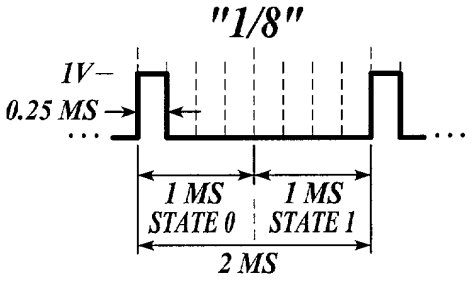

"1/8"
1V
0.25 MS
1 MS
STATE 0
1 MS
STATE 1
2 MS

Fig.3B

DUTY CYCLE	POSSIBLE MODULATOR BINARY OUTPUT COMBINATIONS	TIMER STATE
0% (0/8)	0 0 0 0	0 1
12.5% (1/8)	0 1 0 0	0 1
	0 0 0 1	0 1
25% (2/8)	0 0 1 0	0 1
	1 0 0 0	0 1
	0 1 0 1	0 1
37.5% (3/8)	0 0 1 1	0 1
	1 1 0 0	0 1
	0 1 1 0	0 1
	1 0 0 1	0 1
50% (4/8)	0 0 1* 00	0 1
	1* 00 0 0	0 1
	0 1 1 1	0 1
	1 1 0 1	0 1
	1 0 1 0	0 1
62.5% (5/8)	0 1 1* 00	0 1
	1* 00 0 1	0 1
	1 1 1 0	0 1
	1 0 1 1	0 1
75% (6/8)	1* 00 1 0	0 1
	1 0 1* 00	0 1
	1 1 1 1	0 1
87.5% (7/8)	1* 00 1 1	0 1
	1 1 1* 00	0 1
100% (8/8)	1* 00 1* 00	0 1

* INDICATES OVERFLOW BIT

Fig.4

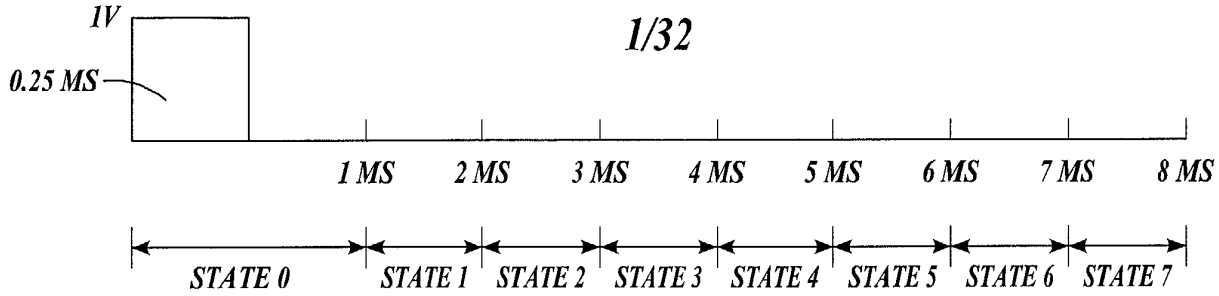


Fig.5A

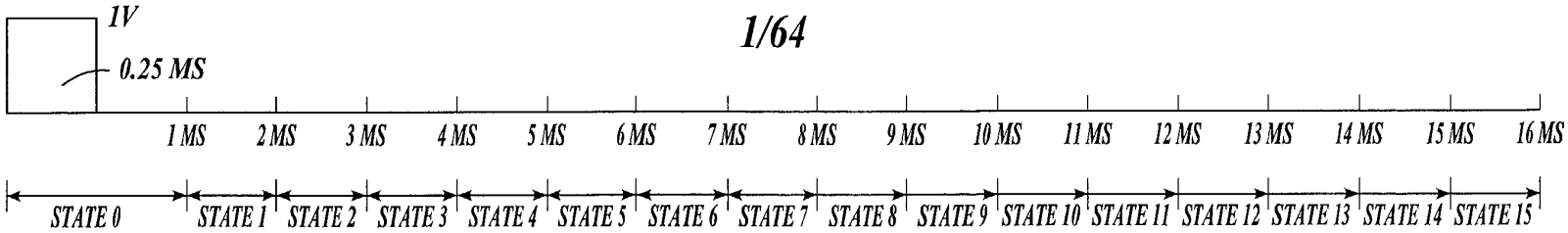


Fig.5B

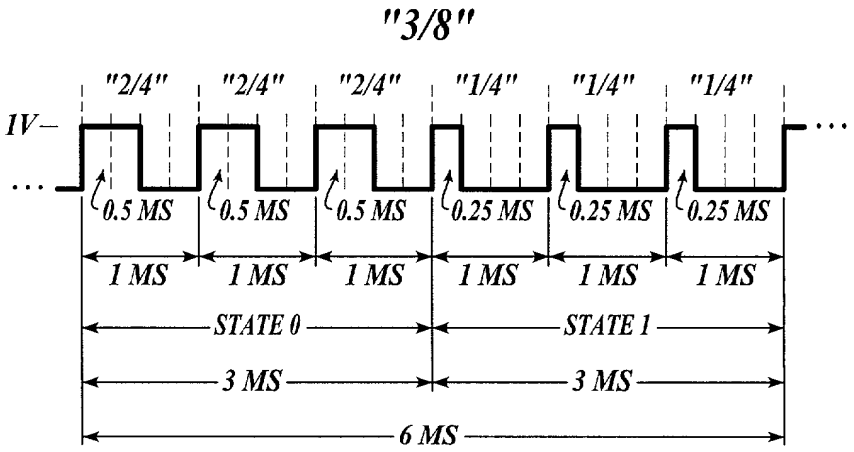
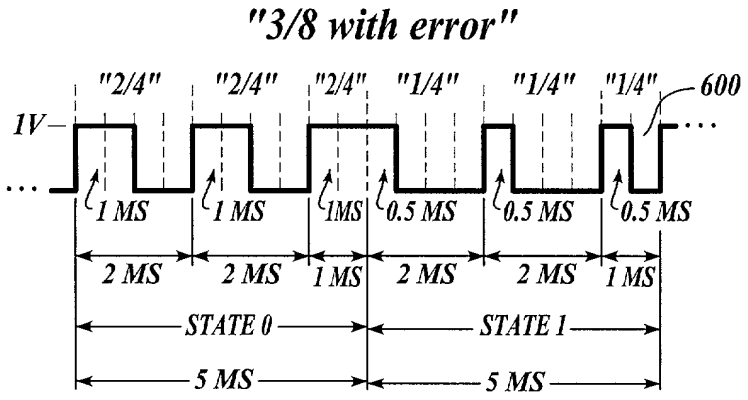


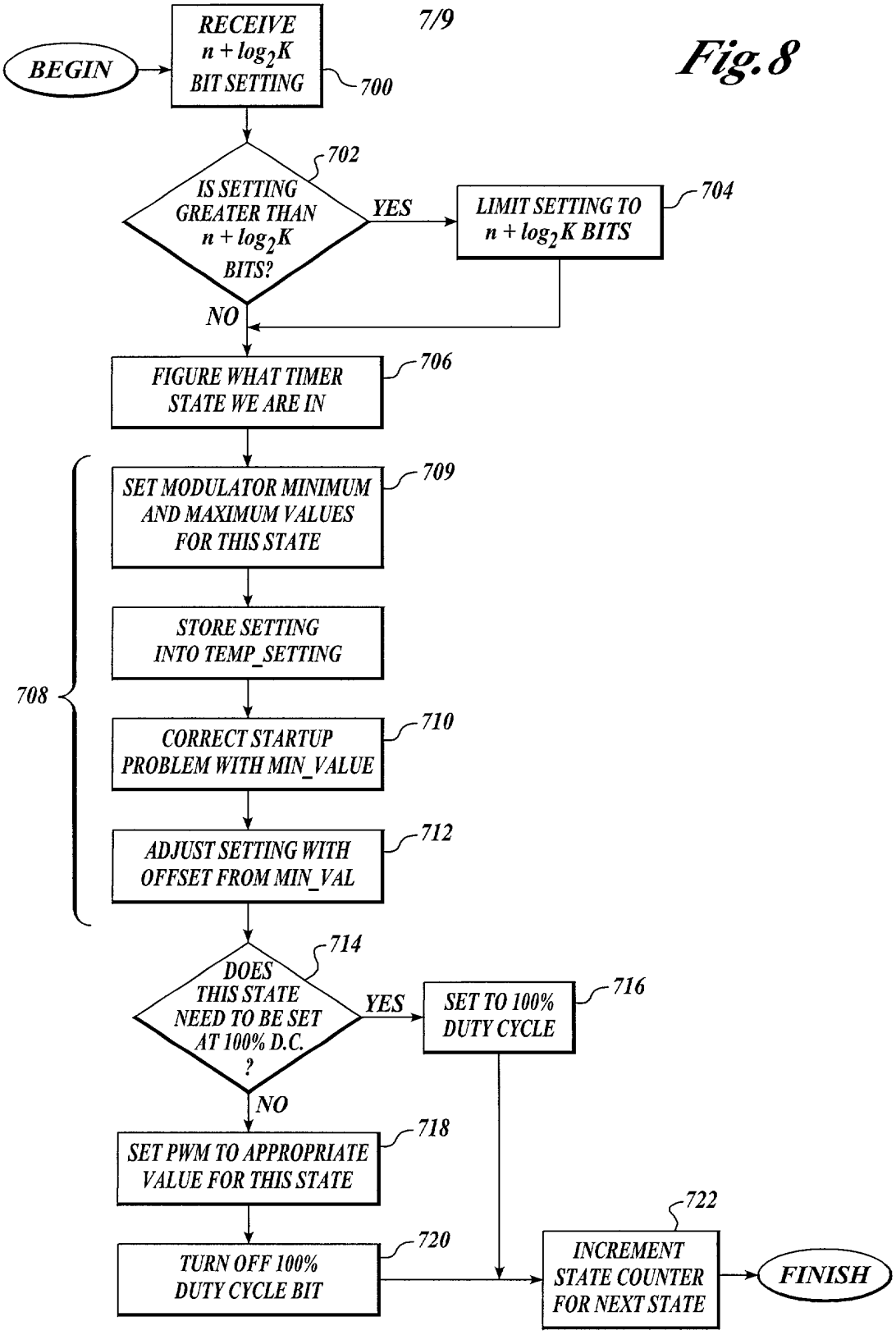
Fig. 6



PWM PERIOD = 2 MS, TIMER PERIOD = 5 MS

Fig. 7

Fig. 8


BEGIN
RECEIVE $n + \log_2 K$ BIT SETTING
700
IS SETTING GREATER THAN $n + \log_2 K$ BITS?
702
YES
LIMIT SETTING TO $n + \log_2 K$ BITS
704
NO
FIGURE WHAT TIMER STATE WE ARE IN
706
708
SET MODULATOR MINIMUM AND MAXIMUM VALUES FOR THIS STATE
709
STORE SETTING INTO TEMP_SETTING
CORRECT STARTUP PROBLEM WITH MIN_VALUE
710
ADJUST SETTING WITH OFFSET FROM MIN_VAL
712
DOES THIS STATE NEED TO BE SET AT 100% D.C. ?
714
YES
SET TO 100% DUTY CYCLE
716
NO
SET PWM TO APPROPRIATE VALUE FOR THIS STATE
718
TURN OFF 100% DUTY CYCLE BIT
720
INCREMENT STATE COUNTER FOR NEXT STATE
722
FINISH

TOTAL PULSE DURATION AS MEASURED IN UNIT PULSE LENGTHS	MODULATOR OUTPUT IN EACH TIMER STATE							
	TIMER STATE							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	0	0	0	1	0	0	0
3	1	0	1	0	1	0	0	0
4	1	0	1	0	1	0	1	0
5	1	1	1	0	1	0	1	0
6	1	1	1	0	1	1	1	0
7	1	1	1	1	1	1	1	0
8	1	1	1	1	1	1	1	1
9	2	1	1	1	1	1	1	1
10	2	1	1	1	2	1	1	1
11	2	1	2	1	2	1	1	1
12	2	1	2	1	2	1	2	1
13	2	2	2	1	2	1	2	1
14	2	2	2	1	2	2	2	1
15	2	2	2	2	2	2	2	1
16	2	2	2	2	2	2	2	2
17	3	2	2	2	2	2	2	2
18	3	2	2	2	3	2	2	2
19	3	2	3	2	3	2	2	2
20	3	2	3	2	3	2	3	2
21	3	3	3	2	3	2	3	2
22	3	3	3	2	3	3	3	2
23	3	3	3	3	3	3	3	2
24	3	3	3	3	3	3	3	3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2040	255	255	255	255	255	255	255	255
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2047	256	256	256	256	256	256	256	256

Fig. 9

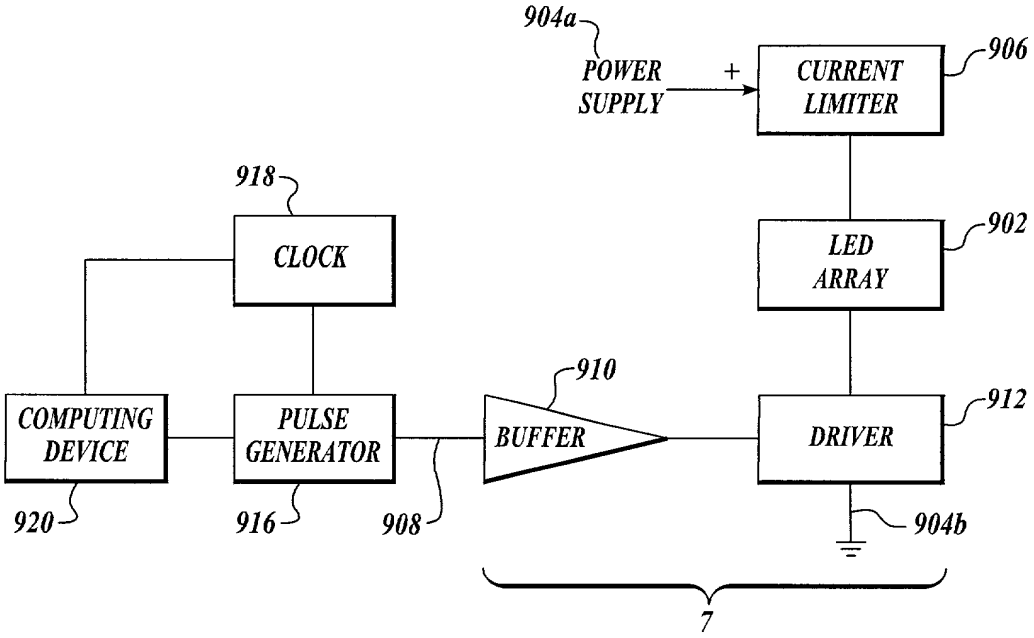

904a
POWER SUPPLY
+
CURRENT LIMITER
906
918
CLOCK
LED ARRAY
902
910
COMPUTING DEVICE
PULSE GENERATOR
BUFFER
DRIVER
912
920
916
908
904b
7

Fig. 10